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[Blocking in Wavelength Routing Networks, Part I: The Single .. - Zhu, Rouskas, Perros \(1999\) \(Correct\) \(7 citations\)](#)

parts of the network, and second, the signal **power** is channeled to the receiver and is not spread to pair in contrast, a uniform traffic **distribution** is assumed in most other studies. Second, our February 17, 1998 Abstract We study a class of **circuitswitched** wavelength routing networks with and <ftp.csc.ncsu.edu/pub/tech/98/TR-98-02.ps.Z>

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[High-Energy Physics on DECPeRLe-1 Programmable Active Memory - Moll, Vuillemin, Boucard \(1995\) \(Correct\) \(5 citations\)](#)

com puting systems fall short either of computing **power**, or of I/O resources or both. 1 Introduction 1.1 features, such as tracks and energy level **distribution** in order to achieve discrimination based on using a Clibrary to describe the synchronous **circuit** to be implemented. This approach allows at the <pam.devinci.fr/pub/doc/LdV/MVB95.ps.Z>

[Self-Timed FPGA Systems - Payne \(1995\) \(Correct\) \(4 citations\)](#)

systems, due to their modularity, robustness, lowpower consumption and averagecase performance. data is passing through the system. No Clock **Distribution** Problems: Problems such as clock skew are main drawback to selftimed systems is that extra **circuitry** is required to generate the local timing <www.dcs.ed.ac.uk/home/rep/selfTimedFPGA/paper.ps.gz>

[Hazard-Free Implementation of the Self-Timed Cell Set in a.. - Maheswaran, Akella \(1994\) \(Correct\) \(1 citation\)](#)

asynchronous systems can result in minimizing **power** dissipation because only components contributing sequential **circuits**. If there exists some **distribution** of stray delays such that a **circuit** may reach to deal with them in gatelevel asynchronous **circuits** are surveyed. Then the lookup table (LUT) model <ftp.ece.ucdavis.edu/pub/akella/fpga95.ps.Z>

[Towards Synthetic Benchmark Circuits For.. - Stroobandt.. \(1999\) \(Correct\) \(1 citation\)](#)

find a solution that obeys both Rent's rule and a **power** law net degree **distribution**. Hence, for the first characteristic Rent curve and the net degree **distribution** of real versus synthetic benchmark **circuits** is Towards Synthetic Benchmark **Circuits** For Evaluating Timingdriven Cad Tools Dirk <www.elis.rug.ac.be/~dstr/ISPD99.ps.Z>

[A Multidisciplinary Optimization Approach to Integrated.. - Lokanathan Jay \(1995\) \(Correct\) \(1 citation\)](#)

the effect of spacing between cells on the **power** and delay were determined to be as shown in as input variables and compute the temperature **distribution** across the package via finite element and Network Sensitivities'IEEE Transactions on **Circuit** Theory, vol. 16, num. 3, August 1969, pp. <www.cse.nd.edu/pub/Reports/1995/tr-95-5.ps.gz>

[Gallium Arsenide Process Evaluation Based on a RISC.. - Brown Senior \(1993\) \(Correct\) \(1 citation\)](#)

means that good speed can be realized with lower **power** supply voltages, giving DCFL a good **powdelay** variable width signal routing, multiphase clock **distribution**, ground planes, and automatic **powerrail** sensitivity of the microprocessor and other large **circuit** blocks to different process parameters is <www-personal.engin.umich.edu/~brown./Publications/12-93.ps>

[Finding Improved Wire-Antenna Geometries with Genetic .. - Van Veldhuizen.. \(1997\) \(Correct\) \(1 citation\)](#)

used as a good compro mise. ffl The amount of **power** used by the sensors when transmit ting a message process. Integral equations for current **distribution** on each wire are formulated, then the

for maximum power transfer from the antenna. Basic circuit design teaches the greatest amount of power is www.afit.af.mil/Schools/EN/ENG/LABS/PARALLEL/Students/dvanveld/icec98.ps.gz

Architecture Evaluator's Work Bench and and its Application.. - Fu, Quach, Flynn (1995) (Correct)

5 Conclusion 26 iii List of Figures 1 Area Versus Power Statistic for Microprocessors :

:13 11 Interconnect length distribution of VLSI chip in 1982 :

SPECfp92 results, and demonstrate the effect of circuit density on FUPA implementations. Key Words and umunhum.stanford.edu/tr/fu.jun95.tr668.ps.Z

Experiments on Flexibilities for Logic and Routing.. - Balakrishna Kumthekar.. (Correct)

as the key determinants of overall performance and power dissipation-the traditional sequential design and route tools are used. Figure 1 shows the distribution of all the circuits after place and route.

of interconnect-fail to deliver after the circuits are placed and routed. We use functional bessie.colorado.edu/~kumtheka/html/papers/iwls99.ps.gz

Intrinsic Area Array ICs: What, Why, and How - Peyman Dehkordi Chandra (1997) (Correct)

of a periphery Structural/Thermal Signal Clock Power/Ground C4 Bumps Passivation Layer Substrate Pads metal layer of the die or on an additional distribution metal layer. The purpose of this paper is to approach, it is possible to design chips around circuit constraints rather than pad constraints that microsys6.engr.utk.edu/ece/mcmc97_2.ps

Development of a DSP/MCM Subsystem Assessing Low-volume.. - Peyman Dehkordi Tim (1996) (Correct)

selected is a 37 mm x 37 mm 5layer (1 pad, 2 power, and 2 routing layers, 62 pitch) MCMD based including all branches was 77.286 mm. The delay distribution on the module is shown in below: percent paths noise, rise/fall times, and coupling noises on circuit networks of arbitrary topology. A typical microsys6.engr.utk.edu/ece/mcmc96_2.ps

An Accurate and Stochastic-Based Approach to Timing-Driven.. - Dutt (Correct)

of choice for optimizing any objective like timing, power and area. We establish desirable characteristics incorporating design constraints (e.g.uniform distribution of wiring across routing channels)and to deep submicron technology, and to the large circuits that are implemented on such chips. We present www.eecs.uic.edu/~dutt./papers/ispd98-2.ps

Minimizing the Effect of Clock Skew Via Circuit Retiming - Brian Lockyear (1993) (Correct)

Minimizing the Effect of Clock Skew Via Circuit Retiming Brian Lockyea

ftp.cs.washington.edu/tr/1993/05/UW-CSE-93-05-04.PS.Z

Combinatorial Aspects of Lower Power Clock Layout Synthesis in.. - Jun Dong (Correct)

Combinatorial Aspects of Lower Power Clock Layout Synthesis in VLSI Synchronous load and switching at high frequency, clock distribution is a major source of power dissipation. Also, Power Clock Layout Synthesis in VLSI Synchronous Circuits Jun Dong Cho Dept. of Electrical and Computer vada.skku.ac.kr/Project/published/clock_lp.ps

Clock-Routing Driven Layout Methodology for Semi-Synchronous .. - Atsushi Takahashi (Correct)

network C may depend on the wiring area, power consumption, and reliability. But it has expensive part in modern VLSIs is the clock distribution network where the clock is assumed to be Driven Layout Methodology for SemiSynchronous Circuit Design 3 Atsushi TAKAHASHI, Wataru TAKAHASHI, ku-www.ss.titech.ac.jp/~atsushi/place-tau.ps

Implications Of Area-Array I/o For Row-Based Placement.. - Caldwell Kahng (Correct)

[15]Peripheral I/O pads also constrain clock/power distribution, and their inherently large

Peripheral I/O pads also constrain clock/power distribution, and their inherently large parasitics cause May Be Correlated With Topological Depth Of Circuits. 1. Introduction Ic Packaging Technologies With nexus6.cs.ucla.edu/~abk/papers/conference/c74.ps

Resume - Shao (Correct)

distribution system design'IEEE Transactions on Power Delivery, Vol. 6, No. 4, pp. 16071615, October and Y. Zhang, An expert system for secondary distribution system design'IEEE Transactions on Power Numerical Computation, Electromagnetic Theory, Circuits and Systems, Electronics Lab, and

www.isr.umd.edu/~jshao/resume/resume.ps

Learning As Applied to Simulated Annealing - Lixin Su [\(Correct\)](#)

or handle a variety of tradeoffs between area, power, and timing, for example. Design technologists of generating a move is referred to as proposal distribution[5]The computation of p, r, and their by learning from the annealing of benchmark circuits. This model is then used in the trained www-cad.eecs.berkeley.edu/~lixinsu/research/paper1.ps

On Ultrametricity in Feedforward Neural Network Error Surfaces - Gallagher, Downs [\(Correct\)](#)

of the nature of the error surface will enable more powerful training algorithms to be developed, and more points were then used to generate the sample distributions described in the previous section. Three problems (e.g, traveling salesman [4]circuit placement [8] and graph colouring [2]1]and www.elec.uq.edu.au/~annis/papers/gallagher_acnn98.ps.gz

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[charge in states collector-controlled and transfer real-space.. - Luryi Serge](#) (Correct)

requencies, structure, 7 speed ultimate The gain. **power** the and current the both for Ghz 40 were the is Charge tails those participate, function **distribution** hotcarrier the of tails highenergy the in the structure, CHINT basic the in Thus, elements. **circuit** novel of implementation the allows have we www.ee.sunysb.edu/~serge/101.ps.gz

[Energy Consumption Management in Design - Smit](#) (Correct)

Abstract-A survey of the basic issues in low **power** design is presented, including techniques for is usually a signal with a random sig nal **distribution**. So the statistics of the remainder are better in the early design phase of analog and digital **circuits**. The concept of energy complexity will be www.stw.nl/programmas/prorisc/workshop/proc/psz/smit1.ps.gz

[Standard Cell Placement For Even On-Chip Thermal Distribution - Ching-Han Tsai](#) (Correct)

dif ferential constraint to its corresponding **power distribution** constraint. Dealing directly with Standard Cell Placement For Even Onchip Thermal Distribution Chinghan Tsai Sungmo (steve) Kang uivlsi.csl.uiuc.edu/~chtsai/Personal/..../Publications/ispd99.ps.gz

[Alewife Systems Memo 24 - Implementation Of](#) (Correct)

:6 2.4 Power distribution :

Alewife machine using one Alewife node per printed **circuit** board. Alewife nodes are processing elements pattern or folded up in card cages. The logical **placement** of the connectors on the board using a mosaic ftp.cag.lcs.mit.edu/alewife-memos/24.ps.Z

[Constructive Algorithms Based on Graph Minors - Govindan, Langston.. \(1997\)](#) (Correct)

advances in the field of graph minors have yielded **powerful** nonconstructive tools to tackle many finding a threetrack gate matrix layout for VLSI **circuits**. We design a streamlined test for a half dozen rows and columns to provide transistor **placement** and interconnections. The columns are realized www.cs.utk.edu/~library/TechReports/1997/ut-cs-97-345.ps.Z

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Page(s): 758 -766

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Roberts, R.K.; Engel, T.W.; Proctor, F.;
Industrial Electronics, Control, Instrumentation, and Automation, 1992. 'Power Electronics and Motion Control', Proceedings of the 1992 International Conference on , 9-13 Nov. 1992
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Proctor, R.; Fox, B.; Flynn, D.;
Electric Utility Deregulation and Restructuring and Power Technologies, 2000. Proceedings. DRPT 2000. International Conference on , 4-7 April 2000
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Buffet, P.H.; Natonio, J.; Proctor, R.A.; Sun, Yu.H.; Yasar, G.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 , 21-24 May 2000
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5 I/O cell placement and electrical checking methodology for ASICs with peripheral I/Os

Yasar, G.; Chiu, C.; Proctor, R.A.; Libous, J.P.;
Quality Electronic Design, 2001 International Symposium on , 26-28 March 2001
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6 Installation of ADSS fiber optic system on Roseville 60 kV transmission line

Proctor, D.O.;
Power Engineering Society Summer Meeting, 2001. IEEE , Volume: 1 , 15-19 July 2001
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7 Water-cooled, high-intensity ultrasound surgical applicators with frequency tracking

Martin, R.W.; Vaezy, S.; Proctor, A.; Myntti, T.; Lee, J.B.J.; Crum, L.A.;
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , Volume: 50 Issue: 10 , Oct. 2003
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Kiamilev, F.E.; Krishnamoorthy, A.V.; Rozier, R.G.; Rieve, J.; Aplin, G.F.; Hull, C.D.; Farbarik, R.; Oettel, R.E.;
Multi-Chip Module Conference, 1997. MCMC '97., 1997 IEEE , 4-5 Feb. 1997
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Rozier, R.; Farbarik, R.; Kiamilev, F.; Ekman, J.; Chandramani, P.;
Krishnamoorthy, A.; Oettel, R.;
Broadband Optical Networks and Technologies: An Emerging Reality/Optical MEMS/Smart Pixels/Organic Optics and Optoelectronics. 1998 IEEE/LEOS Summer Topical Meetings , 20-24 July 1998
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Chowdhury, S.; Breuer, M.;

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2 Planar embedded InP/GaInAs p-i-n photodiode for very high-speed operation

Miura, S.; Kuwatsuka, H.; Mikawa, T.; Wada, O.;

Lightwave Technology, Journal of, Volume: 5 Issue: 10, Oct 1987

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3 Application of Copper Conductor and Ruthenium Containing Oxides-Glass Resistor to High-Frequency Hybrid IC's for a Portable Cellular Radio

Ogawa, T.; Fujii, M.; Asai, T.; Ikegami, A.; Kobayashi, T.;

Components, Hybrids, and Manufacturing Technology, IEEE Transactions on [see also IEEE Trans. on Components, Packaging, and Manufacturing Technology, Part A, B, C], Volume: 11 Issue: 2, Jun 1988

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4 Application of copper conductor and ruthenium containing oxides-glass resistor to high-frequency hybrid ICs for a portable cellular radio

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Tehrani, S.; Nair, V.; Weitzel, C.E.; Tam, G.;
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6 Optimal placement of IEEE 1149.1 test port and boundary scan resources for wafer scale integration

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Burke, P.A.;
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9 Novel TAB inner lead bonding technology eliminating bump formation process

Otsuka, Y.; Kaneko, H.; Sasaki, J.; Itoh, M.; Takekawa, K.; Yoshigai, A.; Urushima, M.;
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10 Effects of die pad anchoring on package interfacial integrity

Nguyen, L.T.; Michael, M.M.;

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11 Solder crack caused by die attach paste

Wakizaka, S.; Kobayashi, M.; Mizuno, M.;

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Hess, C.; Stroele, A.P.;

Semiconductor Manufacturing, IEEE Transactions on , Volume: 7 Issue: 3 , Aug.
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**14 Characterization of high frequency interconnects using finite
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Jong-Gwan Yook; Dib, N.I.; Ratehi, L.P.B.;

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Sept. 1994

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**15 CMOS ESD protection structures-characteristics and performance
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Physical and Failure Analysis of Integrated Circuits, 1995., Proceedings of the
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16 Perforated silicon membranes as an artificial neural contact pad-chip design and tissue implant response

Laurell, T.; Drott, J.; Qing Zhao; Wallman, L.; Montelius, L.; Bjursten, L.M.; Lundborg, G.; Danielsen, N.;

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Ray, J.; Snyder, D.;

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Berger, H.H.; Sturm, J.; Esfahani, F.; Benedix, A.; Von Aichberger, S.; Muller, B.; Hofacker, K.-O.;

Microelectronic Test Structures, 1997. ICMTS 1997. Proceedings. IEEE International Conference on, 17-20 March 1997

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20 Thermal evaluation of a flip chip RF-PA for simulation-driven short-cycle re-design

Teng, S.Y.; Lee, T.-Y.T.;

Electronic Components and Technology Conference, 1997. Proceedings., 47th, 18-21 May 1997

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21 Pixel detector readout electronics with two-level discriminator scheme

Pengg, F.;

Nuclear Science Symposium, 1997. IEEE , 9-15 Nov. 1997

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22 The use of concentrated hydrogen peroxide for the removal of a TiW ARC from aluminum bond pads

Danzi, R.B.; McLaurin, A.;

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Ezawa, H.; Miyata, M.; Inoue, H.;

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24 Surface contamination of bonding pads incapable of Au wire bonding

Watanabe, M.; Tabuse, K.;

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25 The fine pitch direct bonding technology for chip interconnection

Tohyama, H.; Ozawa, S.; Kitayama, Y.; Yamashita, T.; Nakamura, Y.;

IEMT/IMC Symposium, 2nd 1998 , 15-17 April 1998

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26 Pixel detector readout electronics with two-level discriminator scheme

Pengg, F.;

Nuclear Science, IEEE Transactions on , Volume: 45 Issue: 3 , June 1998

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27 A low-power 170-MHz discrete-time analog FIR filter

Xiaodong Wang; Spencer, R.R.;

Solid-State Circuits, IEEE Journal of, Volume: 33 Issue: 3, March 1998

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28 Achieving crack free package through elimination of type II failure

Chai, T.C.; Chan, K.C.; Wong, E.H.; Fan, X.J.; Lim, T.B.;

Electronic Components and Technology Conference, 1999. 1999 Proceedings.

49th, 1-4 June 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) **IEEE CNF**

29 A calibration-free 3.0 V 12-bit 20 MSPS A/D converter

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